CCD CONTROLLER
CTR-A1700

Features
Fully synchronized image acquisition
CIA software supported
4 independent video channels
16 independent bias voltages with telemetry
8+8 fully programmable Hor/Vert phases
7 temperature input channels
Shutter and step motor output
4+4 opto-isolated I/O channels

Applications
Scientific CCD controllers
Astronomy and Spectroscopy
Scientific research

The CCD Controller CTR-A1700 represents the result of 10 years of experience in the field of CCD image acquisition for astronomy and spectroscopy. The CTR-A1700 is composed of the following items (see Figure 1):

- CTR base unit, containing:
  - Correlated Double Sampling board (CDS), for signal conditioning, filtering and A/D conversion of (up to) 4 independent CCD video outputs
  - Sequencer board (SPC), for the generation of phases and pixel processing signals necessary for the control of a wide range of scientific and industrial CCDs
  - CFO board for fiber-optic connection between SPC and host PC
  - Power Supply Unit for CDS/SPC/CFO boards
- PCI Controller Interface board (PCI), mounted inside the host PC, for the remote control of the CDS/SPC boards by means of an optical-fiber transmission link
- CIA software package

CDS Board (see Figure 2)
The 4 channels can be used for the simultaneous control of 4 different CCDs (arrays) or 4 sections of the same CCD. All signals are generated at the same clock rate from a 20MHZ system clock, so as to provide an optimal synchronization between stimulation and output.

The CDS board provides 16 independent bias voltages rails. Bias voltage rails are individually programmable and range from –22V to +22V. By means of the CIA software library, the characteristics of each bias voltage and pixel processing signal can be preset in accordance with

application, CCD requirements, or personal preferences. Each bias voltage is provided with a telemetry circuit for remote control and fine tuning.

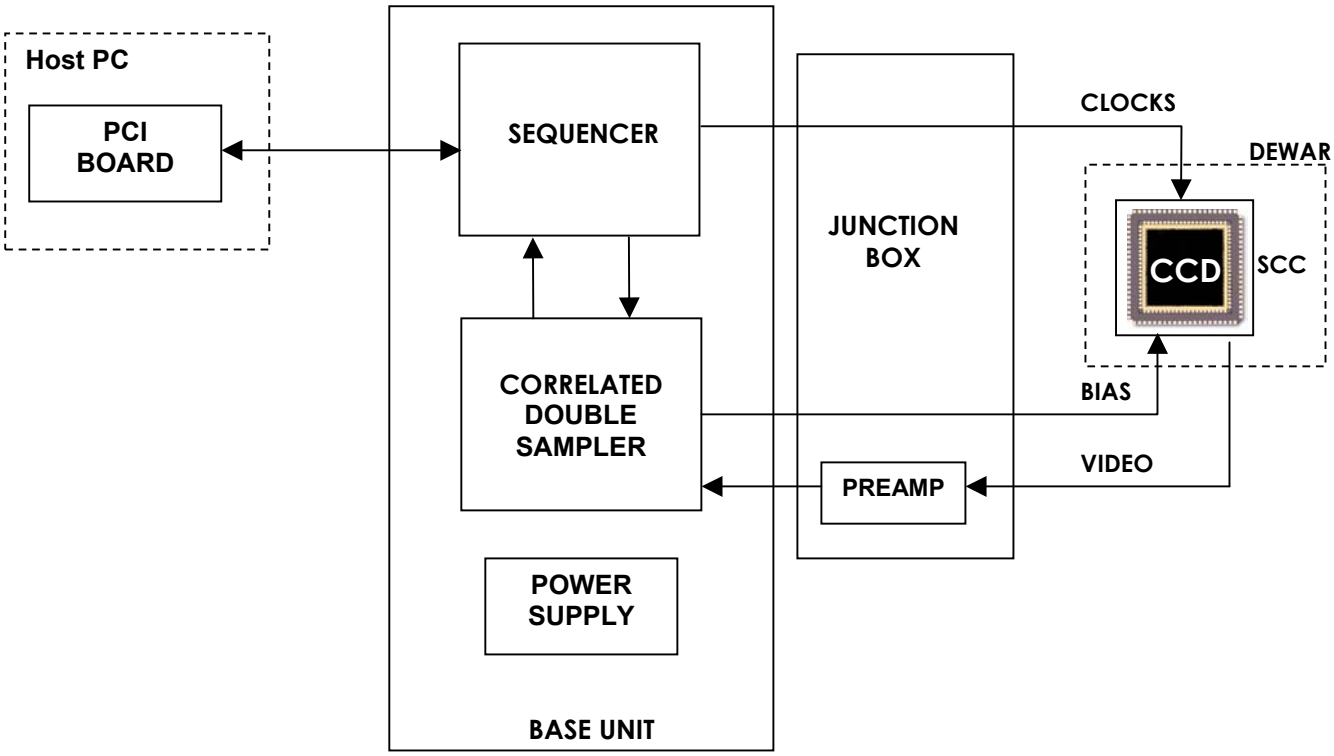

Fig. 1 – Composition of CTR-A1700

The Correlated double sampling circuit is available in many different configurations. In all cases, the CDS input circuitry can be easily optimized, thanks to the following features:

- SW-programmable Clamping voltage
- SW-programmable Offset voltage
- SW-programmable Gain
- SW-programmable Bandwidth

Each input channel can be individually configured.

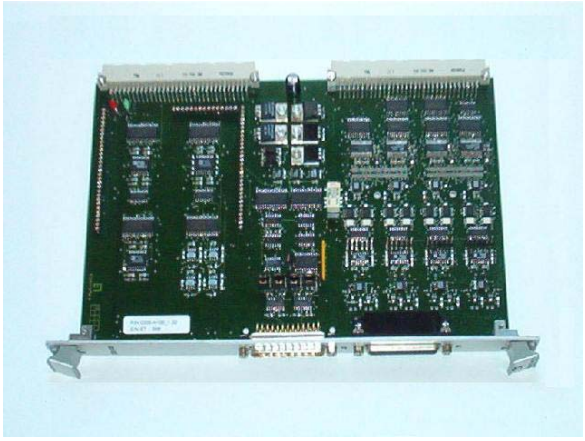

Fig. 2 – CDS Board

SPC board (see Figure 3)

The SPC phases and pixel processing signals are generated at the same clock rate from a 20MHZ system clock, in order to provide an optimal synchronization between stimulation and output. The video output is separately received and processed by one or more CDS boards, synchronized with the same timeline. Up to 8 CDS can be simultaneously controlled by a single SPC.

8 vertical phases and 8 horizontal phases are available: the timing of each phase is independently programmable and can be configured using the simple GUI provided with the CIA software package. The bias voltage rails of the SPC are also software programmable and range from –10V to 10V. By means of the CIA software library, User can preset the characteristics of each phase and pixel processing signal, in accordance with CCD requirements, actual application or personal preferences.

The SPC Sequencer board also provides a number of additional features, useful for the construction of a complete CCD controller:

- thermostatic circuit for an external heater or Peltier cell
- step motor output for shutter control, focus, or others
- 8 optoisolated, SW configurable I/O channels

Fig. 3 – SPC board

CDS - Technical Characteristics

Model	Value			Units	Notes
	min	typ	max		
Video input					
Number of independent channels		4			
Gain		5			SW programmable
Bandwidth		3.5		MHz	SW programmable
Resolution		16		Bit	
Differential input range		±200		mV	
INL			±1	LSB	
Throughput			1	MSPS	4 MSPS total, with all 4 video channels active
Offset	-2.5		+2.5	V	SW programmable
Bias Voltages					
Number of independent signals		16			
Output range	-22		+22	V	
Telemetry		Provided for each channel			

SPC - Technical Characteristics

Model	Value			Units	Notes
	min	typ	max		
Phases					
Horizontal phases		8			optically isolated (A400 only)
Vertical phases		8			
Low rail voltage (VL)	-10		0	V	SW programmable
High rail voltage (VH)	0		+10	V	SW programmable
Resolution		8		Bit	
Rail-to-rail voltage (VH-VL)	2.7			V	
Multilevel phases		3			A400 only
Timing resolution	50			nsec	
State duration	50			nsec	SW programmable
Raising / falling time		1		µsec	independent from rails HW programmable
Telemetry		Present on each signal			
High voltage output	20		50	V	A400 only, SW programmable
Pixel processing					
Number of independent signals		8			
Output		Single-ended or LVDS			
Thermostatic circuit					
High precision temp. channel		1			Designed for 4-wire sensor Used for thermostatic circuit
Gen. Purpose temp. channels		5			Designed for AD590 sensor
Temp. input resolution		12		Bit	
Threshold	-200		+50	°C	SW programmable
Actuator output voltage		24		V	Suitable for heater or peltier cells
Actuator output current			1.5	A	
Shutter					
Switch voltage		24		V	100msec duration
Keeping voltage		15V resistor limited			A400 A100
Expo time resolution		24		Bit	
Expo time duration	100			msec	
Step motor output		4		poles	Optically isolated
General					
Communication link			20	Mpixel/sec	
System Clock		20		MHz	
Input, general purpose		4			Optically isolated
Output, general purpose		4			Optically isolated